Compact high-gain lumped differential 40 Gb/s driver amplifiers in production 0.15 µm PHEMT technology.

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Abstract — **High-performance and very compact 40 Gb/s driver amplifiers were realized in mature 0.15 µm depletion PHEMT technology. The 3-stage lumped differential drivers feature a large differential 40 Gb/s output swing of up to 7.5 V_{pp}, RMS jitter of less than 800 fs, rise and fall times of less than 10 ps and more than 27 dB gain. The small size (1.4x1.7 mm) and ability to have DC coupled in- and output, enable compact and cost-effective optical 40 Gb/s long-haul transmitters with system grade NRZ and RZ eyediagrams.**

I. INTRODUCTION

One of the main challenges in building a long-haul 40 Gb/s optical transmitter is the realization of a driver amplifier with 6-8 V peak-to-peak (V_{pp}) output swing, required to fully modulate the external $LiNbO_3$ or GaAs Mach-Zehnder modulator (MZM). Mainly single-ended distributed driver amplifiers have been proposed in literature sofar [1-3]. Such amplifiers require very precise bypassing of the power supplies and AC coupling or RF chokes at the output. While distributed amplifiers deliver excellent bandwidth, their single-stage gain is typically not high enough to directly interface between the 40 Gb/s multiplexer, often realized in SiGe, and the modulator. Therefore, often a cascade of two or more AC coupled amplifiers has to be used, increasing transmitter complexity, size and power consumption.

In this paper, we report compact, high gain differential 40 Gb/s driver amplifiers implemented in mature production 0.15 µm PHEMT technologies. These lumped three-stage drivers can be DC coupled at in- and output and have a differential voltage output swing of up to 7.5 V_{pp} at 40 Gb/s, RMS output jitter of less than 800 fs, rise and fall time less than 10 ps and more then 27 dB differential gain.

II. CIRCUIT DESIGN

Circuits were fabricated in both 3- and 6-inch 0.15 µm depletion PHEMT foundry processes, each having a transit frequency f_T of about 100 GHz, maximum oscillation frequency f_{MAX} of about 160 GHz and a gate-to-drain breakdown of at least 8V, sufficient to provide the 4V single-ended output swing needed for the output FET.

The relatively low f_T of a 0.15 µm PHEMT makes the design of a lumped 40 Gb/s amplifier with sufficient linear bandwidth very challenging. However, a driver amplifier typically operates under compressed output swing conditions, such that the digital eye quality is determined not only by bandwidth but mainly by the non-linear limiting behavior. In this respect, distributed topologies potentially show an increase in jitter due to non-uniform clipping along their in- and output transmission lines.

A schematic diagram of the lumped driver amplifier is shown in figure 1. It features three differential stages, each consisting of a differential inverter preceded by one or two source-followers to transform the impedance and shift down the DC level using level shifting diodes. The input stage has on-chip 50 Ω resistors to provide good input match. As the input needs to be DC coupled to the –0.6V to 0V CML output swing of the multiplexer, an additional positive voltage supply (V_{cc1} of 1.5V) is used to increase the drain-source voltage of FET in the input source follower. Different peaking methods for lumped designs have been suggested in literature [4] to improve to pulse rise and fall times. Here, only small inductive peaking at the first two inverter loads is used to minimize the impact of peaking on jitter performance. A cascode topology is adopted for the output stage to improve the bandwidth by reducing the Miller capacitance and resulting RC time constant. As the output common-gate FET of the cascode requires enough voltage headroom, the 75 Ω output loads needed to provide the output modulation current are tied to a second positive supply (V_{cc2} of 5-7V) resulting in a common mode output voltage of about 0 V enabling DC coupling of the driver to a 50 Ω terminated MZM. By changing the current in the output stage (VOA), the output swing can be modulated between 4 and 8 V_{pp}. The output swing control also allows to automatically set the bias point of the MZM using a low-frequency AM modulation tone technique. Finally, the design also contains sense and feedback resistors to enable automatic DC offset cancellation using an off-chip operational amplifier. Offset cancellation is required when using HEMT technology, because the high gain and spread of the threshold voltage V_T, will typically lead to unbalanced differential outputs.

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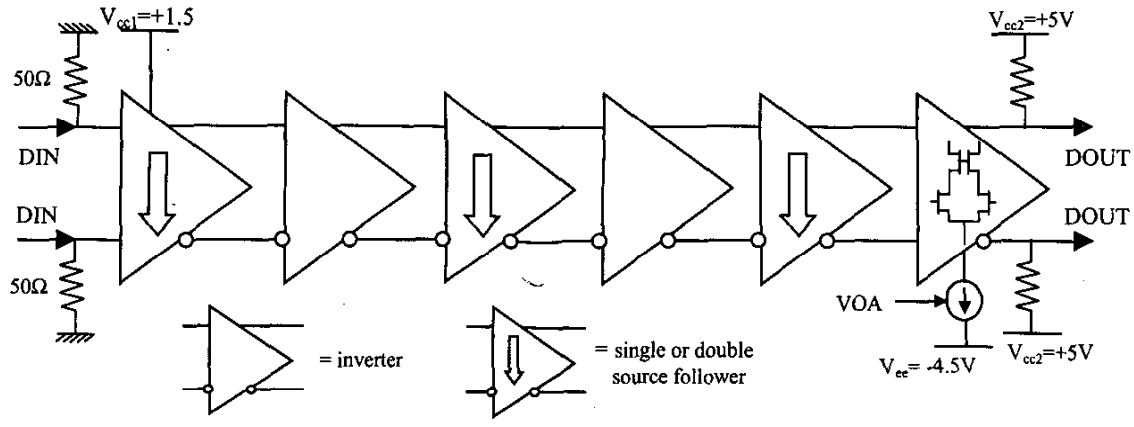

Fig.1: Schematic diagram of the 3-stage lumped driver amplifier (feedback loop for automatic offset control not shown)

The layout of the lumped amplifier is shown in figure 2. A completely symmetric layout was adopted with short connections between the sources of the differential inverter pairs. To enhance the stability of the design, a large number of via holes through the 100 µm thick microstrip substrate provide low-inductance grounding and connections at the output of source followers were kept as short as possible. RC bypass networks were used at different power supplies. The total chip size is 1.43 by 1.73 mm^2.

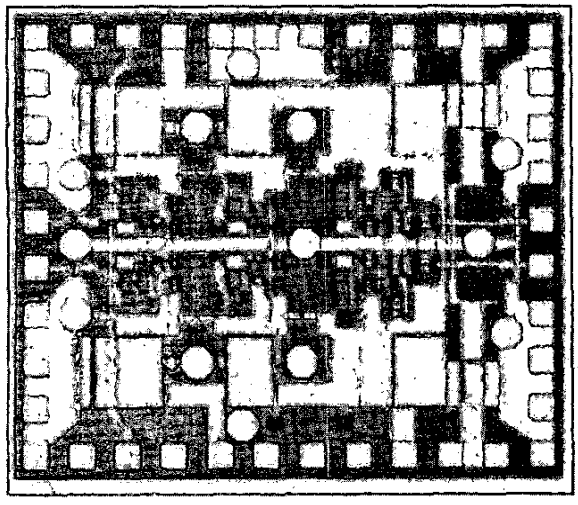

Fig. 2: Chip photograph of the lumped PHEMT driver.

III. CIRCUIT RESULTS

The on-wafer measured S-parameters of a lumped driver with inductive load peaking are shown in figure 3. Typical bias conditions are 450 mA from the main -4.5V supply, 20 mA from the +1.5V and 120-150 mA from the +5V supplies, adding to a total DC power dissipation of 2.5-3 W. A 3-dB bandwidth of 27 GHz and 28 dB differential gain are obtained together with good input matching.

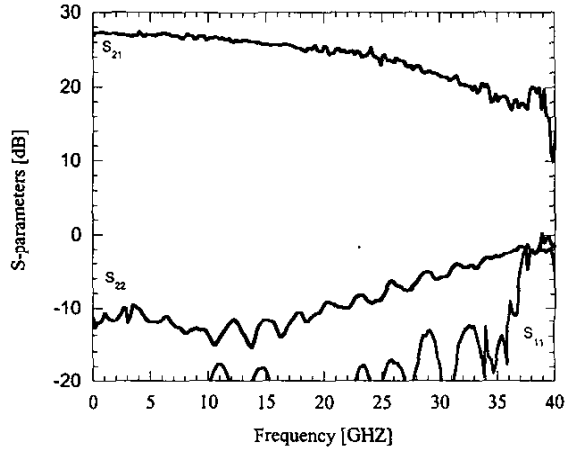

Fig. 3: On-wafer measured S-parameters of lumped driver (single-ended to single-ended measurement, 6 dB was added to gain to reflect differential gain).

One of the drawbacks of the lumped output buffer design is clearly the deterioration in output reflection at higher frequencies (>20 GHz) caused by the capacitive output impedance of the common gate FET in parallel with the 75 Ω output loads. However, when assembling this die, part of this capacitance can be compensated by the inductance of the short output bondwire.

Electrical eyediagram measurements were performed using 2^{31}-1 PRBS pattern generated by a 4-channel 10Gb/s pattern generator and 3 external 2:1 HEMT multiplexers, resulting in a 40 Gb/s differential output swing of 1-1.2V_{pp}. Critical for a good on-wafer electrical eye measurement is that connections between source and amplifier and especially between the driver amplifier and the oscilloscope samplers are kept as short as possible. Therefore detachable samplers heads were used connected to the GSSG output probes using a short cable.

The on-wafer measured 40 Gb/s electrical eye diagrams are shown in figure 4 and 5, respectively for a driver with output biased for maximum clipping and for maximum swing (7.5 V_{pp} differential). For both cases, excellent eyes are obtained with short rise and fall times (<10 ps, 20-80%) and clean eye rails resulting from the limiting behavior of the driver and small difference between static and dynamic swing. While these are single-ended measurements, a very good symmetry is observed. The output jitter is about 800 femtosecond RMS (<4 ps peak-to-peak), which is identical to the input jitter caused by the preceding 2:1 multiplexer.

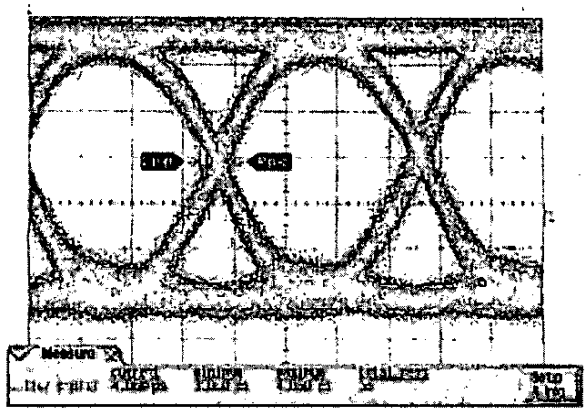

Fig 4: On-wafer measured 40 Gb/s eyediagram of PHEMT driver (Vertical scale: 0.5V/div, eye shown single-ended). The amplifier was biased for maximal clipping. Differential output = 5.5 V_{pp} for differential input ~ 1 V_{pp}.

The drivers were integrated together with 16 to 4 and 4 to 1 multiplexers, based on SiGe, and an external 20 GHhz VCO into a small multilayer ceramic module. Apart from HF capacitors to provide a parallel bypass for some of the power supplies no external components were needed enabling a very short differential coplanar connection between multiplexer and driver and from the driver to the GPPO output connectors leading to the Mach-Zehnder modulator.

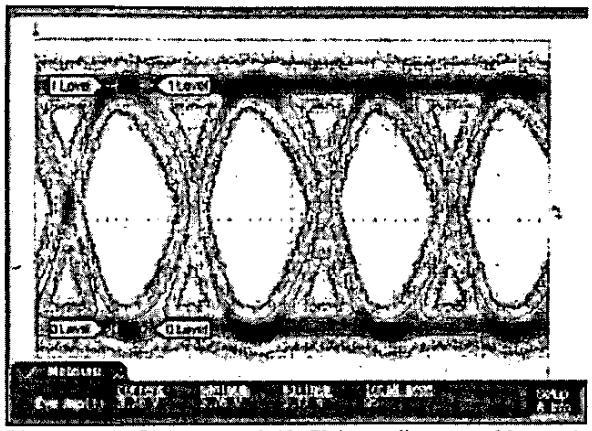

Fig 5: On-wafer measured 40 Gb/s eyediagram of lumped PHEMT driver (Vertical scale: 0.7V/div, eye shown single-ended). Amplifier biased for maximal output swing. Differential output = 7.5 V_{pp} for differential input ~ 1 V_{pp}.

The optical 40 Gb/s NRZ eyediagram of a complete module is shown in figure 6. Again, excellent eyes with clean rails are obtained. These high-speed circuit packs will also be used for long-haul 40 Gb/s WDM applications. In such long-haul transmission typically an RZ format is used together with forward-error-correcting code (FEC), increasing the transmitted bitrate to 42.7 Gb/s. An example of an optical 42.7 Gb/s 33% RZ eyediagram generated using our integrated module driving the data stage and a high-power 21.3 GHz VCO driving the pulse stage of a dual-stage Mach Zehnder Modulator is shown in Figure 7. Please note that the bandwidth of the optical sampler used for this measurement is only 50 GHz, which introduces some distortion for 42.7 Gb/s 33 % RZ measurements.

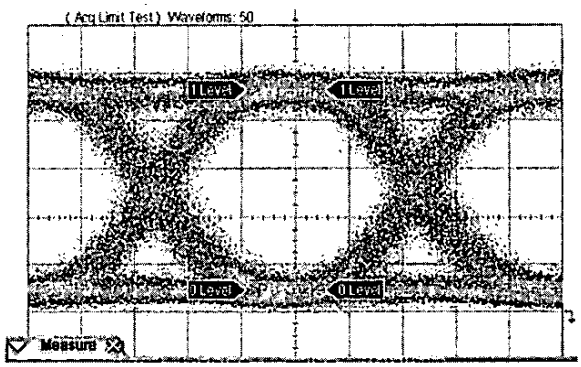

Fig. 6: Optical 40 Gb/s NRZ eyediagram of integrated module consisting of SiGe MUX and GaAs PHEMT driver driving $LiNbO_3$ Mach-Zehnder modulator.

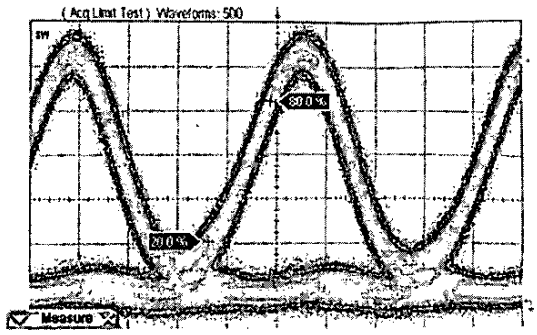

Fig. 7: Optical 42.7 Gb/s RZ eyediagram of integrated module consisting of SiGe MUX and PHEMT driver.

IV. Conclusion

In this paper, we have shown for the first time the feasibility of making very compact DC-coupled 40 Gb/s MZM driver amplifiers using a purely lumped design in a mature 3- or 6-inch PHEMT production technology. While many of the published 40 Gb/s driver eyediagrams often do not show enough margin to be used in real system applications, we have demonstrated both electrical and optical eyes with low jitter, clean rails and fast rise and fall times.

A further improvement in bandwidth and rise- and fall times which will be needed for 80 and 100 Gb/s optical systems could be obtained using InP D-HBT technology [5].

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